

Efficiency Improvement of a Wireless Power Transfer System

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Abstract: The efficiency of the power transferred through coupling is most critical in low power on-chip Wireless Power Transfer (WPT) systems. Various techniques can be used to improve this efficiency and reduce the losses at multiple stages of the design. Efficiency improvement starts with selecting proper resonant transfer topology according to design requirements. The mixed model leads to approx. 39% improvement in efficiency for comparable loads (loads with impedance similar to that of LC tank). To reduce rectifier losses a voltage multiplier circuit, using lvt-NMOS (low threshold NMOS) based switches, can be implemented instead of rectifying diodes, which provides 25% increase in DC efficiency. Further improvement in efficiency can be achieved by transmitting a high Peak-To-Average-Power-Ratio (PAPR) signal for faster switching of rectifying devices; simulation results show 11% more efficient system when using chaotic signals (which have the highest PAPR) rather than using single-frequency continuous wave.

Keywords: Wireless Power Transfer (WPT), resonance, coupling models, coupling coefficient (k), RF-DC converter, rectifier-less conversion, high peak-to-average-power-ratio (PAPR) signals.

I. INTRODUCTION

Wireless Power Transfer is a technique widely used for many applications including implantable medical devices [1][2], Radio Frequency Identification (RFID) tags [3], energy harvesting [4] etc. The loss of power during wireless transfer and conversion to DC signal is quite high and dictates a low efficiency. There are various techniques used at all stages throughout the WPT design chain, to obtain higher efficiency.

The first step is to design the transmitter and receiver LC network according to the requirements. For this the most preferred is resonant transfer due to its high efficiency [5]. The various resonant models are discussed and compared below.

The LC network is followed by the rectifier for AC-to-DC conversion. This is where the major power loss occurs, reducing the overall efficiency. Many researchers are focusing on improving the rectifier design for minimum efficiency loss [6]. Others are focusing on altogether removing the rectifier and using other conversion techniques such as a voltage multiplier [7].

This work focuses on such a design where the rectifier is replaced by a switch-based modified converter, which is driven by timing signals, generated by the WPT receiver. Further explanation is provided in Section-III Part-2.

Another area explored for efficiency improvement is the transmitter side. While using a rectifier and feeding a modified signal from transmitter end [8] rather than just a pure sinusoidal signal, leads to higher efficiency.

II. CONVENTIONAL WPT SYSTEM

The main components of the conventional WPT system are shown in Fig.1. The first and foremost

elements of this chain are the Transmitter-Receiver (TX-RX) coils, which are responsible for the electromagnetic transfer of energy. This transfer can take place using pure inductive coupling [9], capacitive coupling [10] or resonant coupling [11]. The latter is the most widely used technique due to its property to provide increased power transmission at a certain resonant frequency [12].

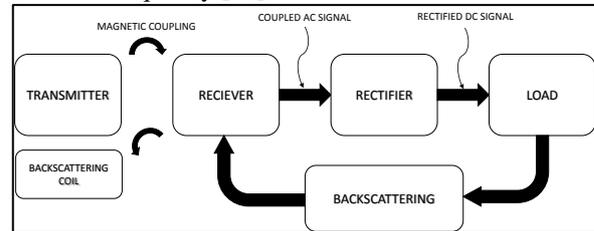


Fig.1. Conventional WPT System Block Diagram

Since the element responsible for coupling losses are the coils, for improving efficiency researchers are focusing on designing a high Q inductor by improving coil design and using various shielding methods [13].

The next major step is to convert the received AC signal to the required DC level. This step is performed by a rectifier consisting of self-timed switching elements such as diodes. During the rectification process these devices incur a voltage drop to turn-on. This aspect considerably reduces the rectifier efficiency. This effect is especially dominant in miniature on-chip receiver designs.

Backscattering communication is used to transmit the data back to the external coil. An extra external coil, placed beside the primary external TX WPT coil, resonating at the switch frequency, receives this excitation with high-selectivity due to resonance. This approach is based on the scheme shown in [6] where an

external separate coil is used for back-scattering communication, operating at a lower frequency than the WPT frequency. In [7], the author has proposed extracting a clock from the coupled power-signal, divide the extracted clock frequency using simple cascades-of-DFF (D-Flip Flop) and then use it as a carrier for back-scattering communication.

III. TECHNIQUES FOR IMPROVING WPT EFFICIENCY

1. ENHANCING QUALITY FACTOR OF ELECTROMAGNETIC COUPLING

Electromagnetic coupling is used to transmit high power with higher efficiency [16]. According to maximum power transfer theorem, maximum power is transmitted when the impedance of reactive circuits (inductors and capacitors) is at its minimum. This occurs during resonance. Resonance is the phenomenon during which the inductive and capacitive impedances become equal and cancel each other's effect, resulting in overall minimum impedance equal to the resistance of the circuit.

While improving efficiency the resonant transfer also impedes some disadvantages. The phenomenon of resonance takes place exactly where the capacitive and inductive impedances cancel each other. If there are even slight changes in the on-chip capacitance due to manufacturing process, this can lead to a shift in the resonance frequency. Hence this results in degradation of the quality factor at the working frequency. This effect can be tackled by keeping a capacitive bank for tuning and providing frequency selection [7].

An important factor that is critical in the performance of the WPT circuit is the coupling coefficient (k). This coefficient is dependent on various parameters of the design, including inductor size, working frequency, distance between the TX and RX side, the current through the coil, the resistance of the conductor wire of inductor (R_{series}), and other structural parameters. One way to improve coupling is to design High-Q on-chip inductors, though these methods involve expensive post-processing techniques [17][18].

RESONANCE COUPLING MODELS

The phenomenon of resonance is shown to provide increased efficiency [19] therefore it is the widely opted method for WPT; using either of the below mentioned coupling models.

A. Series coupling model

For series coupling circuits (Fig.2a) the power source used at transmitter should be a voltage source to provide maximum power for transmission.

Series resonance coupling models are used for lighter loads [14]. When a lighter load is connected in series with the inductor and capacitor, the overall impedance

of the circuit will be closer to the impedance of the LC tank. This minimizes the effect of load on resonance. For this case the load should be much smaller than the capacitive impedance.

B. Parallel coupling model

For parallel coupling model (Fig.2b) the power source used at the transmitter should be a current source.

In case of heavy loads parallel topology is preferred, because resulting impedance of the parallel combination will be closer to the resonant impedance of the LC tank, thereby not disturbing resonance [14].

C. Mixed coupling model

Mixed coupling models (Fig.2c) provide better impedance matching as compared to series and parallel coupling models. Better impedance matching will eventually result in better resonance coupling. For efficient wireless power transmission through long distances, using magnetic coupling, mixed coupling models are preferred for better results [15]. Apart from impedance matching mixed coupling also provides efficient WPT for a large range of frequencies (kHz to MHz) [20].

This model is specially preferred when the load impedance is comparable to the capacitive impedance of the circuit. In this case the matching is better achieved through a combination of series and parallel LC networks.

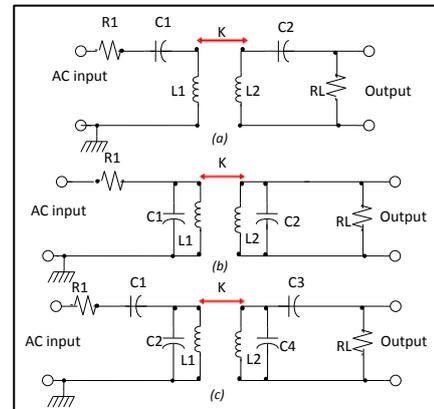


Fig.2 (a) Series coupling model (b) Parallel coupling model (c) Mixed coupling model

D. Simulation Results

For simulation purposes, arbitrary values of RLC components are used to study the different topologies. The software used is *Virtuoso*, *Cadence Inc*. The frequency of signal transfer used is 200MHz.

As discussed the mixed model leads to improved efficiency in case of comparable load size. The capacitive impedance in this case is 1.2kilo-ohms, and hence for the load kept as 1kilo-ohms, it can be classified as comparable load. At this load size the mixed model proves most efficient. The efficiency is 39% improved when using mixed model with a reasonable coupling coefficient ($k=0.2$), as compared to parallel

topology. The effect of this model is even more dominant in case of low coupling (i.e. for smaller 'k' such as 0.05). (Refer Table.1 (iii) (iv))

When the load size is smaller than the capacitive impedance then series LC coupling model provides highest efficiency (Table.1 (i) (ii)). While for large loads parallel topology gives better efficiency (Table.1 (v) (vi)).

Table.1: Comparison table of coupling models

	Parameters		Efficiency (%)		
	k	RL(ohms)	Series	Parallel	Mixed
i	0.05	50	55	2	50
ii	0.2	50	87	5	35
iii	0.05	1k	7	28	53
iv	0.2	1k	54	67	93
v	0.05	50k	0.2	87	80
vi	0.2	50k	2	56	9

2. ELIMINATING RECTIFIER FOR EFFICIENCY IMPROVEMENT

Since the rectifier leads to efficiency loss during AC-DC conversion, there is a recent trend towards "rectifier-less" design, eliminating the rectifier from the chain and using other approaches for the AC-DC conversion. One such technique is to utilize a multi-stage voltage multiplier as in [7] instead of rectifier. The circuit in [7] makes use of self-timed devices, incurring a sufficient drop in efficiency.

The proposed technique in this work is shown in Fig.3. The theme is to avoid a rectifier while producing the required DC voltage. A conventional rectifier utilizes self-timed diodes in bridge configuration, using the concept of inverting the current direction in one half of a cycle, thereby resulting in Direct Current through the load for complete cycle. Even though the self-timed devices are useful as they do not require any control signals, the drawback is the loss of power. This loss occurs because of the drop that is essential to overcome the threshold for turning on these self-timed devices.

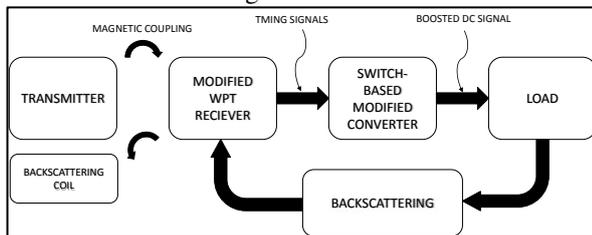


Fig.3. Modified WPT system for efficiency improvement

The capacitors at each stage of the voltage multiplier (shown in Fig.4a) are used to boost the voltage level and convert the AC current to DC. The switches used are lvt-NMOS (low threshold NMOS). This enables these devices to switch on much faster with fewer losses as compared to the diode threshold loss.

The first stage of the design is a clamper, comprising

of two switches; pre-charge and feed-forward lvt-NMOS switches, controlled by timing information from the WPT receiver. This may be succeeded by a similar second stage which further boosts the voltage level. During these stages the alternating current is converted to DC current and eventually this charge is stored across a large capacitor.

Considering a single stage circuit, when real switches are used, their control signals (i.e. the timing signals generated by modified WPT receiver) need to be quite high to adequately switch them ON, with reasonably low R-ON (the resistance of the switch when it is ON). In order to avoid having to use quite high amplitude of the timing signals, the feed-forward switch (the one which requires the high control signal) can also be bootstrapped as shown in Fig.4b. This eliminates the requirement for extremely high amplitudes of control signals.

The voltage multiplier may be followed by a clamper circuit for protection from exceeding voltage levels [7].

The simulation results of comparison of this technique (using two stages) with the conventional rectifier shows an increase in the DC level achieved of about 25%, as shown in Fig.5.

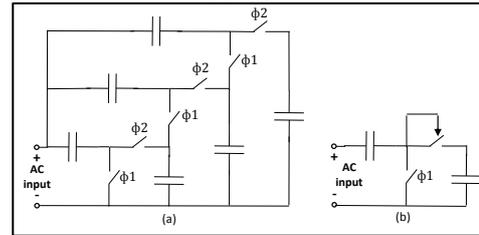


Fig.4. (a) Voltage multiplier circuit using switches instead of diodes (b) Modified single stage

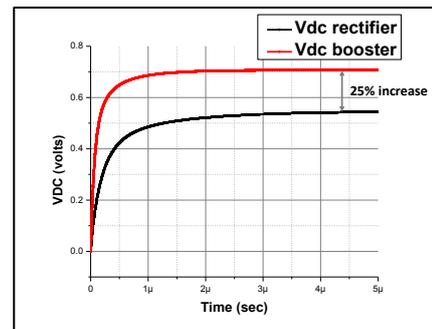


Fig.5. Rectifier and Booster output DC level

3. IMPROVING EFFICIENCY FROM TRANSMITTER SIDE

While a lot of effort has been put into improving the efficiency of rectifiers for WPT, recent trends [8][21] have also focused on using a high PAPR(peak-to-average-power-ratio) waveforms (such as multi-sine, wide-band-noise, chaotic signals, Orthogonal frequency-division multiplexing signals) for transmission. These high PAPR waveforms employ multi-frequency components enabling faster switching

of the feed-forward elements in a rectifier or a voltage-booster just after the secondary coil in a WPT-RX. Therefore, faster switching increases the efficiency of the WPT, especially for low power levels.

When using a multi-sine wave instead of a single carrier sinusoid, this generates power having comparatively higher peaks. When this coupled signal at the receiver is passed through the rectifying diodes, the higher voltage peaks helps to overcome the diode threshold more efficiently. Then these peaks are able to retain more power and are able to charge the capacitors (followed by the rectifier) to a higher level, leading to an increased DC level achieved.

Compared to a single tone signal, the multi-sines, white noise, OFDM and chaotic signals can enhance the efficiency at the output of the rectifier because of their better edge-rates enabling higher-speed switching of the feed-forward elements in rectifiers or gain-boosting stages. The greater the PAPR of the signal is, higher will be voltage peaks received at the secondary coil. As suggested in [8], chaotic signals can embody a considerably higher PAPR than a sine-wave and therefore achieve >20% improvement in rectifying efficiency.

Table.2 summarizes the simulation results of chaotic versus single-sine-wave. After performing simulations it was observed that the efficiency obtained for chaotic signal is approximately 11% more than in case of single sine-wave (these simulation were performed using a large load at low power levels).

Table.2: Comparison table of chaotic vs. sine wave

	Chaotic	Sine Wave
Pin	100mW	101mW
Pout	18mW	7mW
Efficiency	18%	7%
PAPR	10dB	4dB

IV. CONCLUSION

Efficiency losses are most critical in WPT and the recent research is focusing on reducing these losses at various stages in the WPT system.

The model to be used for electromagnetic transfer depends upon a number of parameters, load size and coupling being the two most important among them. The mixed model of resonance, which is a combination of both series and parallel LC network, is most suitable for values of load that are closer to the equivalent impedance of capacitance. The efficiency improvement in this case is about 39%. This model can also be utilized for low coupling between transmitter and receiver.

To overcome the power losses of rectifier, an approach proposed in this work is to use a voltage multiplier circuit instead of the conventional rectifier, driven by timing signals, generated by the modified WPT receiver. This leads to 25% increase in efficiency.

Another approach to improve efficiency is to transmit a high PAPR signal from the transmitter, rather than a

sine wave, resulting in faster switching of the rectifying devices. Transmitting a chaotic signal (which has the highest PAPR) leads to an overall efficiency of 11% more than in the case of sinusoidal signal.

Utilizing these efficiency improvement techniques, as per requirement for an on-chip WPT system, will lead to better performance, as depicted by the simulation results.

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