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A novel Topology of Symmetric Multilevel Inverter

Ashraf Yahya[1,2 *] and Syed M. Usman Ali[3]

[1]Research Scholar, Department of Electronic Engineering, NED University, Pakistan

[2]Asst. Prof, Department of Electronics & Power Engineering, PNEC-NUST, Pakistan (ayahya@pnec.nust.edu.pk)*
Corresponding author

[3] Professor, Department of Electronic Engineering, NED University, Pakistan

Abstract: Multilevel Inverter is industrial standard for Medium Voltage (MV) and High Voltage (HV) applications such as FACTS, HVDC, MV AC motor drives and renewable Energy conversion systems. It produces a higher power-quality output and reduced power losses but requires more hardware than the conventional SPWM inverter. Reduction in the required hardware by means of introducing new topologies has been a focal point of contemporary research in this field of study. This paper proposes a new topology for Cascaded Multilevel Inverter (CMLI) that requires minimum number of IGBT/MOSFET switches and less number of DC sources as compared to a number of topologies recently presented. Working of the proposed topology is validated by means of simulation in Matlab-Simulink.

Keywords: Multilevel Inverter, topology, Total Harmonic distortion (THD).

I. INTRODUCTION

In general, any DC-AC converter (inverter) that produces three or more output levels is termed as Multilevel Inverter (MLI). Conventional Inverters are two-level inverters which can produce only two levels (Square wave) and therefore carry large number of unwanted High frequency sinusoidal components, called Harmonics. The associated power losses in converter switches reduce converter efficiency. Harmonics are shifted to high frequency band by means of carrier based Sinusoidal Pulse-width modulation (SPWM) so that they can be easily filtered out. MLI, on the other hand, produces more output levels and form a stepped waveform closely matched to a sine wave. Power quality is even better when number of steps or levels is increased. In Cascaded Multilevel Inverter (CMLI), single phase H-bridges are cascaded and each H-bridge cell requires a separate DC source. Nevertheless, it requires less number of IGBT/MOSFET switches than other basic MLI topologies, such as Diode-clamped (DCMLI) and Flying Capacitor (FC) [1]. Therefore, most of the researches are focused on CMLI topology, to minimize hardware requirement than a basic CMLI requires. Reduction in number of switches decreases on-state and switching Power losses and therefore increases converter efficiency as well as reduction in converter cost.

II. CMLI TOPOLOGIES

The basic CMLI topology works on chain-link format, where a single H-bridge with its input DC source (Battery/ PV cell/ Fuel cell/ rectified ac) constitutes a link or cell or module. This module can produce +V,0, and –V levels at output. When more such cells are connected in series and a particular switching pattern is applied, it generates stepped output with both positive and negative polarities. In addition, its modular design allows easy replacement and service continuity. Fig.1 presents basic CMLI structure. There are two types of CMLI: symmetric topology where all DC sources voltage and all switches in H-bridge cells are identical, and Asymmetric topology, in which DC source voltages are set by 2^n (binary) or 3^n (Ternary), "n" being the cell or module number(n=0,1,2,3….). Asymmetric topology therefore also requires variety of IGBT/MOSFET switches. With Asymmetric topology, more levels may be produced than with symmetric topology, with the same number of components [2]. The modularity feature however is lost and it requires maintaining variety of stocks of hardware component. Hence for practical needs and manufacturing ease, symmetric topology is more preferred [3].

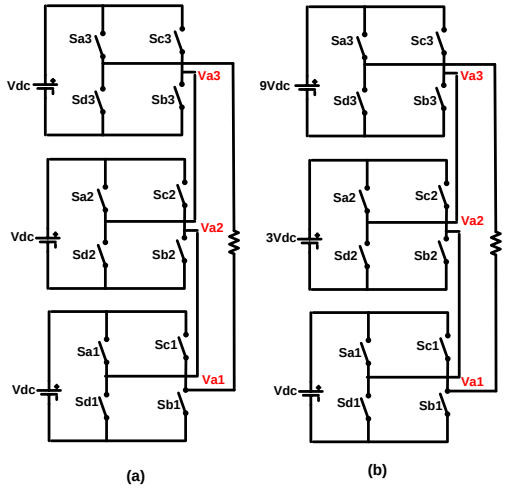

Fig., 1 Basic CMLI topology Symmetric & Ternary

In recent years, many new topologies for both symmetric and asymmetric structure have been presented [4]-[8]. In [5] the CMLI has two sections: level generation (sub-multilevel cells) and polarity generation (H-Bridge) part. As level generation section is composed of switches of low voltage ratings, high frequency modulation strategies can also be applied whereas output stage H-bridge being high voltage and high power stage is switched at power frequency. This topology considerably reduced the total switch count. Topology in [6] further reduced the switch count. A recent improvement is presented in [7] which use two types of cells: single voltage and double voltage sources and in a way is partially symmetric as variety of cells components is introduced. The overall switch count is however less compared with other topologies.

III. PROPOSED TOPOLOGY

A new symmetric topology is presented in this paper with the aim of minimizing the switch count, improved efficiency, manufacturing ease and availability of redundant switch states for charge balancing.

A. Structure

Our proposed topology employs a base unit or cell of a specific voltage and all add-on cells are of double voltage. As will be shown, this topology results in minimum requirement of switches compared with many other symmetric topologies. Each cell uses two switches: one for cascading its voltage source to other modules and second switch for bypassing the whole cell. The output stage uses a reversing switch, an H-bridge, for polarity reversal. Fig. 2 presents the general structure of our proposed topology.

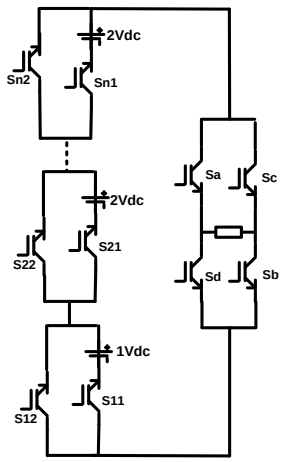

Fig. 2 Basic structure of single phase proposed topology

If "b" represents base cell of voltage V_{dc} and "d" represents number of add-on modules of Voltage $2V_{dc}$, then number of levels "l" produced by the inverter is

$$l = 4\mathrm{d} + \mathrm{b} + 2 \quad (1)$$

$d =$ double voltage cell $= 1,2,3 \ldots..$

$b =$ basic cell $= 1$

And total number of switches "S" used is given by

$$S = 2(d + b) + 4 \quad (2)$$

Whereas the maximum inverter output voltage is the sum of all voltage sources of individual cells.

$$V_{max} = V_{b+} \sum_{n=1,2,3..} nV_d \quad (3)$$

This also gives the blocking voltage rating of H-bridge switches in the output stage.

B. Work description

Switches in each cell of level generation block operate with complementary logic as given in Eq. (4) for "k_{th}" cell

$$S_{k1} = \overleftarrow{S_{k2}} \quad (4)$$

When cascading switch S_{k1} turns on, the bypass switch S_{k2} is turned off simultaneously. Thus voltage of k_{th} cell is cascaded with any previously on cell. Required output polarity is realized by the output H-bridge. Table 1 lists the switching states of an 11-level inverter of proposed topology, as shown in Fig.3. Here with base unit of 50V, two add-on modules of 100V are cascaded to synthesize stepped sine wave output.

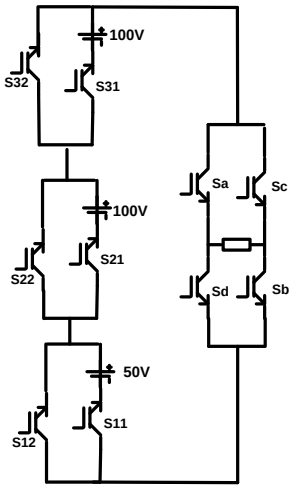

Fig. 3 single phase proposed topology for 11-level inverter

Table 1 Switch states of 11 level inverter switches

V-load	S11	S21	S31	Sa	Sb	Sc	Sd
0	1	0	0	1	0	1	0
50V	1	0	0	1	1	0	0
100V	0	1	0	1	1	0	0
150V	1	1	0	1	1	0	0
200V	0	1	1	1	1	0	0
250V	1	1	1	1	1	0	0
-50V	1	0	0	0	0	1	1
-100V	0	1	0	0	0	1	1
-150V	1	1	0	0	0	1	1
-200V	0	1	1	0	0	1	1
-250V	1	1	1	0	0	1	1

1= ON State, 0=Off state ; Sk1=NOT(Sk2)

It can be observed that in the above Table, the duty ratio of switch S31 is relatively less. This may cause charge unbalance as DC sources of other modules will discharge quicker. However, any level may be generated by various switch combinations and these redundant switch states may be chosen to balance DC source utilization of all cells.

C. Comparison with other topologies

The effectiveness of proposed topology may be determined by comparing it with other topologies in terms of switch count, number of DC input sources. Comparison is made considering output levels and switch count relationship. It is pointed out that more levels generated for equal number of switches means better power quality output of inverter, as Total harmonic distortion (THD) is reduced.

$$THD = \frac{\sqrt{{V_0}^2 - {V_{01}}^2}}{V_{01}} \qquad (5)$$

Table 2 Presents component count of various topologies and proposed one. It is found that our proposed topology requires least number of Switches for generating specific number of levels. The topology is also compared for requirement of DC sources for producing same number of levels; proposed topology also shows superior performance in this contest, as shown in Table 2. Fig.4 shows this comparison in graphical form.

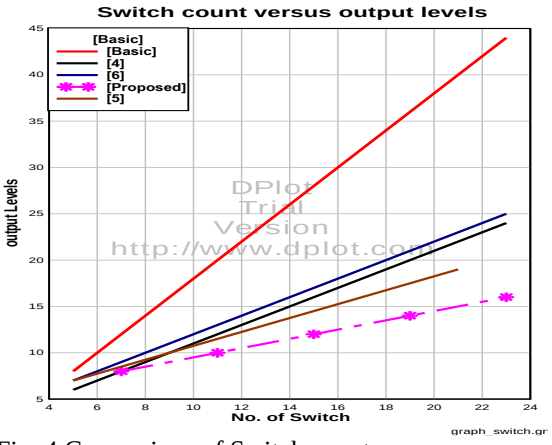

Fig. 4 Comparison of Switch count

Table 2 Components count of various CMLI topologies

	[Basic]	[4]	[5]	[6]	[Proposed]
Number of Cells	n	n	n	n	n
	4	4	4	4	4
DC sources (SDC)	n	n	2n	n+1	n
	4	4	8	5	4
Number of Levels (*l*)	2n+1	2n+1	4n+1	2n+3	4(n-1)+3
	9	9	13	11	15
No. of Switches (S)	4n	2(n+1)	3n+4	2n+5	2n+4
	16	10	16	13	12

IV. SIMULATION RESULTS

The proposed topology is validated by simulations in Matlab-Simulink. A single phase 11-level proposed MLI using a base cell of 50V and two add-on cells of double voltage i.e., 100V are used to model and validate the inverter design. The strategy applied here uses fundamental switching frequency for minimizing converter losses and a number of harmonics are eliminated by Selective Harmonic elimination (SHE) algorithm [9] for the proposed inverter. For fundamental frequency switching, the switching angles for first five levels are calculated iteratively with MATHCAD software. All subsequent angles can be calculated using waveform symmetry. In this study,5th, 7th, and 11th, harmonics are selected for elimination Fig.5, shows the simulation results of 11-level single phase inverter, using Matlab-Simulink. Results show all selected harmonics are completely absent in the output, no DC value and the total Harmonic Distortion is just 10.68% while fundamental output voltage peak is 240V. However, 3rd, 9th and other tripling harmonic magnitudes are higher. This problem is addressed in a

three phase –three wire inverter where all in-phase triplin harmonics are automatically canceled.

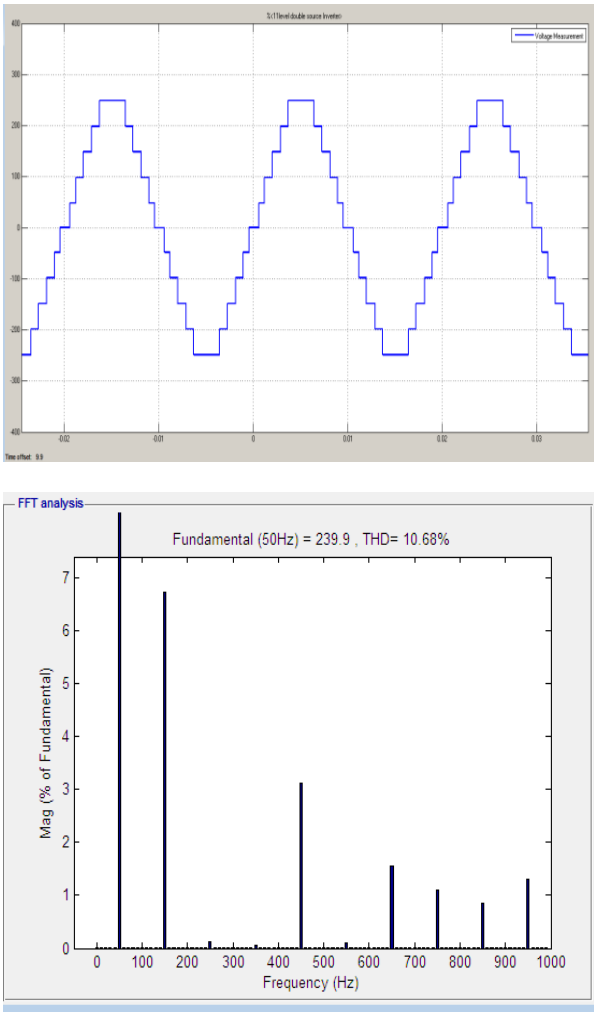

Fig. 5 Simulation result; output voltage & Harmonic profile

V. CONCLUSION

A novel topology for symmetric Cascaded Multilevel Inverter based on all double- voltage source modules proposed in this paper showed improved performance over existing topologies. It requires less number of switches and minimized hardware; so reduced inverter losses and improved efficiency.

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